A 10-Gb/s 275-fsec Jitter Cryo-CMOS Charge-Sampling CDR for Quantum Computing Application

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Abstract— This letter presents the first clock and data recovery (CDR) system operating at 4.2 K designed for quantum computing (QC) applications. By considering the benefits and challenges of cryogenic operation, a dedicated analog CDR structure is employed so as to maintain high performance at 300 and 4.2 K. The CDR incorporates a new complementary charge-sampling phase detector (PD) that achieves low power and low jitter. Fabricated in 40-nm CMOS, the proposed CDR operates at 10 Gb/s, achieving a recovered clock jitter of 260 fs and a jitter tolerance of 2 UI$_{PP}$ at a 5-MHz jitter frequency while consuming 4.7 mW at room temperature (RT). At 4.2 K, the power consumption reduces to 3.1 mW with a recovered clock jitter of 275 fs and a jitter tolerance of 0.85 UI$_{PP}$ at a 5-MHz jitter frequency, demonstrating its functionality for a high-speed cryogenic wireline link.

Index Terms— Charge-sampling phase detector (PD), clock and data recovery (CDR), cryogenic CMOS (cryo-CMOS), full-rate, low jitter, PD.

I. INTRODUCTION

CLOCK and data recovery (CDR) is a crucial block in many established wireline applications. A relatively new application is quantum computing (QC), where cryogenic electronic interfaces have been proposed to address the scalability and the sheer interconnect complexity required to control/readout the thousands of quantum bits (qubits) needed to execute practical quantum algorithms [1]. As shown in Fig. 1, a high-speed cryogenic CDR is required to interface between the controller operating at cryogenic temperature (CT) and the classical algorithm running in a digital processor at room temperature (RT). Considering an envisioned surface code cycle time of ∼1 μs for spin qubits [2], such a CDR should at least support 3-Gb/s data rate to instruct the controller to choose one of eight possible instructions[1] for each of the 1000 physical qubits.

The distinguishing aspect of a CDR is the phase detector (PD). Linear phase detection in high-speed CDRs can be

[1]Having eight instructions per qubit is expected to be sufficient, as any quantum circuit can be *efficiently* implemented using a typical universal set of quantum gates (i.e., H, T, S, and CNOT) and a limited auxiliary set of *X/Y* rotations [3].
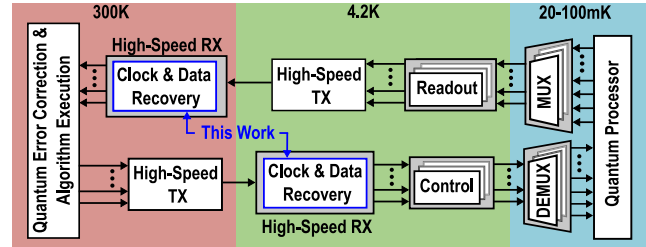

Fig. 1. Simplified block diagram of a scalable QC system incorporating a cryo-CMOS high-speed wireline link.
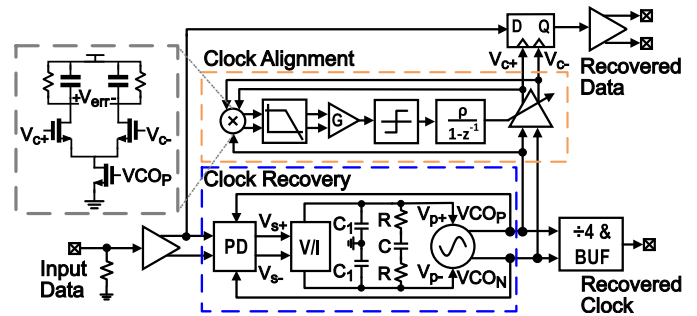

Fig. 2. Proposed CDR architecture.

implemented using a pulse generator in combination with a mixer [4]. While the gain of this PD is high and constant over process, voltage, and temperature (PVT) variations, such a high-frequency pulse generator has a relatively large power consumption (P_{dc}). At CT, a low P_{dc} is crucial due to the limited cooling power available. To reduce P_{dc}, [5] realized a PD using charge steering latches rather than the conventional current steering technique. However, it recovers the data in return-to-zero (RZ) format, adding circuit complexity to convert the data back to non-RZ (NRZ). A more power-efficient approach is presented in [6] by utilizing a master–slave sampler as PD, simultaneously allowing for a wide loop bandwidth and low data-dependent jitter. However, this structure cannot be used directly at CT since its gain is a function of a transistor ON-resistance and the input voltage of its voltage-controlled oscillator (VCO), which varies considerably over the temperature. Moreover, due to the increased threshold voltage at CT [7], the samplers' ON-resistance around mid-rail is relatively high, leading to a degraded loop bandwidth and jitter.

To improve on those limitations, we introduce a complementary charge sampling PD integrated into a cryogenic CMOS (cryo-CMOS) CDR that achieves the lowest reported jitter thanks to its low pattern-dependent jitter and high phase-detection gain.
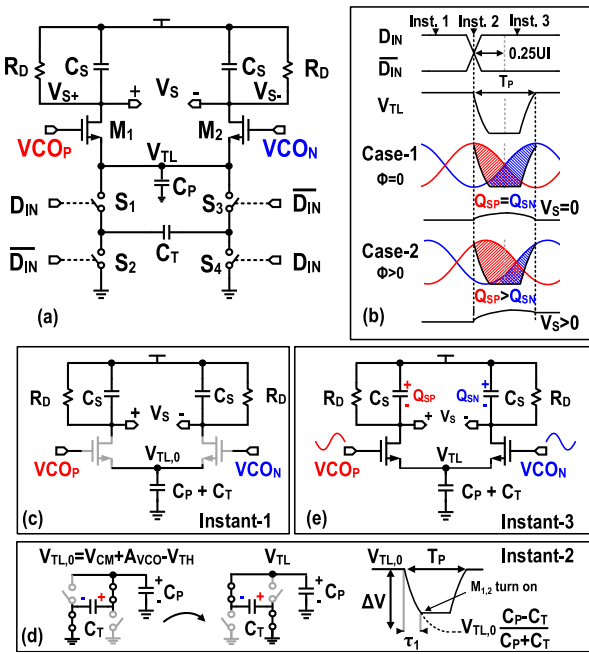
Fig. 3. (a) Schematic and (b) conceptual waveforms of the proposed PD; its simplified schematic (c) before, (d) during, and (e) after a data transition.

II. PROPOSED CRYO-CMOS CDR

Fig. 2 shows the proposed CDR architecture. The incoming single-ended data are converted to differential and drive the complementary charge sampling PD. The PD outputs a differential voltage $V_S(=V_{S+} - V_{S-})$ based on the phase error between the incoming NRZ data and the VCO output $V_O(=\text{VCO}_P - \text{VCO}_N)$. The V/I stage converts V_S into a differential current and injects it into the loop filter, generating tuning voltage V_P $(=V_{P+} - V_{P-})$ to control the VCO. The type-II loop locks the VCO to the data edges with a 0.25-unit interval (UI) offset and prevents major variation of the absolute locking point over PVT variations. A digital calibration loop then shifts the VCO outputs by an additional 0.25 UI to center the retiming edge, optimizing the jitter tolerance of the system.

A. Complementary Charge Sampling PD

Fig. 3(a) and (b) shows the proposed PD and its *conceptual* waveforms. Switches S_{1-4}, tail capacitor C_T, and the parasitic capacitance C_P on the tail node are responsible for generating narrow pulses at the edges of the incoming data to recover a spectral component at the data rate. Transistors $M_{1,2}$ and the load impedance consisting of sampling capacitors C_S and resistors R_D are mainly employed to generate an output voltage based on the phase difference between the data edges and the resampling clock.

At instant-1 in Fig. 3(c), right before a data transition, the current in $M_{1,2}$ is 0 and the tail node voltage $V_{\text{TL},0}$ is high. The charge stored on the tail node capacitance is equal to $(C_T + C_P)V_{\text{TL0}}$, as shown in Fig. 3(d). As the data transition occurs, the polarity of C_T is flipped through S_{1-4}. Consequently, the tail node voltage, V_{TL}, exponentially drops with a time constant of $\tau_1 = 2R_{\text{ON}}C_P$, where R_{ON} is the on-resistance of S_{1-4}, and would reach $V_{\text{TL0}}(C_P - C_T)/(C_T + C_P)$ if the circuit conditions remained unchanged. However, after $\sim 1 \times \tau_1$, V_{TL} is low enough that $M_{1,2}$ turn on and start recharging C_T and C_P, eventually generating the rising edge of the sampling period. The

combination of the discharging due to the polarity flip and the immediate start of the recharging by $M_{1,2}$ generates the sampling pulse, T_P, at the tail node at every data transition, as illustrated in Fig. 3(d). The duration of T_P is determined by the strength of $M_{1,2}$ and the size of C_T, where a transistor results in a shorter pulse duration.

During T_P, the PD schematic simplifies to the one shown in Fig. 3(e). $M_{1,2}$ converts the VCO's output voltage, $\text{VCO}_P - \text{VCO}_N = 2A_{\text{VCO}} \cdot \cos(\omega_{\text{VCO}}t + \phi)$, into a differential current, thus creating a charge difference $Q_S = Q_{\text{SP}} - Q_{\text{SN}} \propto \int_0^{T_P}(\text{VCO}_P - \text{VCO}_N)dt$, on the sampling capacitors as $R_D \gg 1/(C_S\omega_{\text{VCO}})$ [8]. As shown in case-1 in Fig. 3(b), if the VCO zero crossings are at the center of T_P, the integrated charge Q_S is zero since the shaded red and blue areas are equal. Hence, V_S remains zero at the end of the phase comparison, and the CDR is locked. When a phase error ϕ is present, the zero crossings are not centered, and consequently, both Q_S and V_S are nonzero, indicating that the CDR is unlocked [see case-2 in Fig. 3(b)]. During a phase comparison, the output CM voltage of the PD experiences a drop. Hence R_D is added to set the CM voltage of the output by charging C_S between data transitions. After the sampling period, V_S also partially discharges through R_D, resembling the PD to a leaky integrator.

By following a similar approach as [9], the PD gain, K_{PD}, can be estimated by $2\alpha G_M A_{\text{VCO}} R_D \sin(0.5\omega_{\text{VCO}}T_P)/(\pi)$, where G_M is the large signal transconductance of $M_{1,2}$, α (≈ 0.5) the data transition density. Due to the sinusoidal dependence of K_{PD} to T_P, K_{PD} is maximized when $T_P = 0.5T_{\text{bit}}$ and varies negligibly (i.e., less than 5%) even if T_P varies from 0.4 to $0.6T_{\text{bit}}$, where T_{bit} is the bit period.

It is also instructive to investigate the impact of a mismatch between PD's components on its gain and locking point. First, since K_{PD} is not a function of C_S, the locking point is not sensitive to the mismatch between the sampling capacitors. However, a mismatch between load resistors (ΔR_D) and also transistors (ΔG_M) will create a nonzero output voltage if the VCO zero crossings occur at the center of T_P. Consequently, the loop must shift the locking point to compensate for ΔR_D and ΔG_M and realize $\overline{V_S} = 0$ in the locked state. Based on Monte-Carlo simulations, the dominant factor in the locking point shift is due to ΔG_M rather than ΔR_D. $M_{1,2}$ are sized $(W/L)_{1,2} = 4.8$ μm/160 nm, considering the more pronounced mismatch at CT [10]. This limits the 3σ variation of the CDR locking point to ± 2.5 ps.

Switches S_{1-4} and capacitor C_T are sized to roughly adjust T_P to $0.5T_{\text{bit}}$. Even with relatively small switches (i.e., $(W/L)_{S_{1-4}} = 2.4$ μm/40 nm), the falling edge of T_P can be kept short (~ 10 ps), allowing the PD to operate at data rates up to 25 Gb/s. At CT, the resistance of an unsilicided poly resistor reduces by $\sim 10\%$ [1] and G_M increases by $\sim 20\%$–30% due to higher carrier mobility [11]. To maintain a high K_{PD} of 0.3 V/rad over these variations, the PD resistor is 3-bit trimmable around ~ 7.5 kΩ. By considering the tradeoff between the loop phase margin and CM voltage drop, a C_S of 40 fF is chosen. Thanks to its compact switches and charge-based operation, the PD exhibits an extremely low in-band phase noise of -150 dBc/Hz and consumes only 0.1 mW, including the switch driver, while operating at 10 Gb/s.

Fig. 4(a) shows the PD's tail node voltage overlaid for a pseudorandom bit sequence (PRBS). Due to the random interval lengths between data transitions, the node voltage is
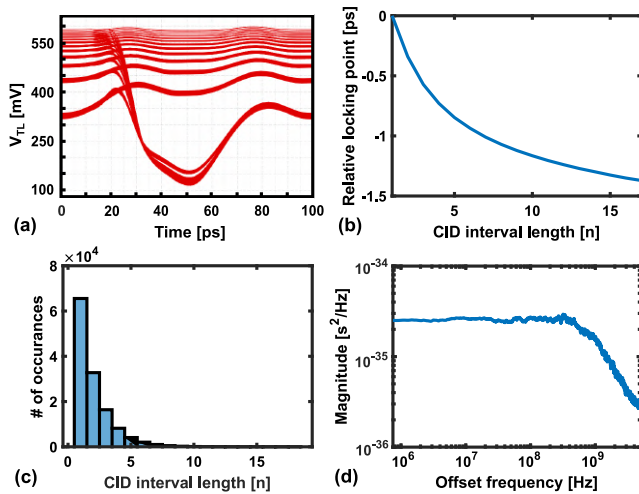
Fig. 4. (a) Simulated tail waveform over many bits of a PRBS17. (b) Relative locking point offset for different data transition densities. (c) Consecutive identical bits in a PRBS17. (d) PD jitter PSD due to its data dependency.
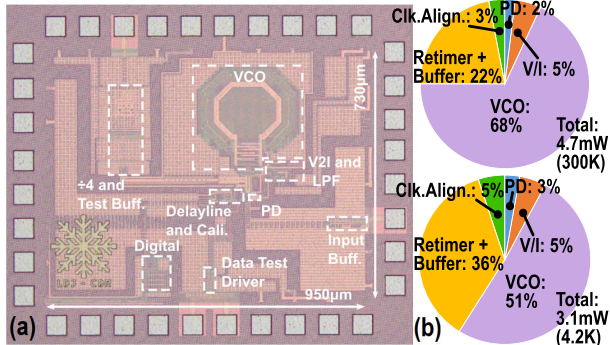

Fig. 5. (a) Chip micrograph. (b) Measured power breakdown at RT and 4.2 K.

higher when no transition has taken place for a longer time. This slightly alters the shape of T_P and, consequently, the absolute locking point, as shown in Fig. 4(b). For a given PRBS, one can determine the number of occurrences of each consecutive identical digit (CID) interval length and assign the weighted value locking point to the sequence, illustrated in Fig. 4(c). The power spectral density is then obtained by performing a fast Fourier transform. By integrating the spectrum shown in Fig. 4(d) over the bandwidth of 40 MHz, an extremely low pattern-dependent RMS jitter of 34 fs is achieved, thus making this structure suitable for ultra-low jitter applications.

B. Clock Alignment Calibration

The clock edges must occur in the center of the incoming bits to maximize CDR tolerance to intersymbol interference (ISI) and jitter. However, the proposed complementary charge-sampling PD locks the VCO zero-crossings 0.25 UI prior to the ideal point. Therefore, as shown in Fig. 2, a phase alignment loop is introduced to shift the sampling clock edges by 0.25 UI (or 90°) and align them to the center of the incoming bits, thus optimizing the jitter tolerance. A mixer-based PD is chosen for this loop as its average output settles to zero when a 90° phase shift exists between its input signals. A low-pass filter suppresses the high-frequency components of the PD output, and the resulting baseband error voltage is then amplified and quantized. The loop filter is implemented by a digital integrator and accordingly adjusts the delay of a controllable delay line consisting of two inverters and a
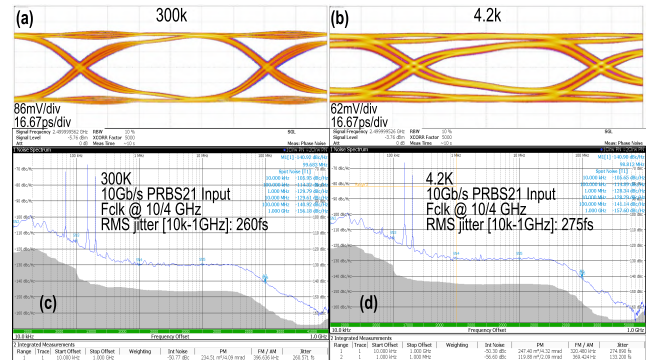

Fig. 6. 10 Gb/s recovered data eye diagram at (a) 300 and (b) 4.2 K. Measured phase noise of the recovered clock at (c) 300 and (d) 4.2 K.

switched capacitor bank in between. The digital delay line also acts as a clock buffer for the retiming flip-flop. The digital integrator operates at ∼1 MHz, provided by an external clock source. Due to the low speed of the loop, all components, excluding the buffer, consume ∼130 μA.

III. MEASUREMENT RESULTS

The cryo-CMOS CDR was fabricated in 40-nm CMOS and occupies an active area of 0.13 mm², as shown in Fig. 5(a). The chip is wire-bonded to a PCB and characterized at 300 K with short cables (∼10 cm). To measure the performance at 4.2 K, the PCB is mounted to one end of a dipstick and lowered into liquid helium. The incoming data is generated at RT by the Keysight M8195A arbitrary waveform generator (AWG). The recovered clock is driven from an ON-chip divider to an R&S FSWP8 to characterize the recovered clock phase noise. A 50 Ω driver transmits the retimed data to RT to characterize the bit error rate (BER) and jitter tolerance. The channel loss due to the cable and PCB trace at 5 GHz is 6 dB. The CDR has a frequency-locking range of ±50 MHz and is optimized separately at 300 and 4.2 K. The CDR core dissipates 4.7 and 3.1 mW from a 1.1 V supply at 300 and 4.2 K, respectively, and its power breakdown is shown in Fig. 5(b). The VCO's power consumption reduces at 4.2 K due to the higher inductor's quality factor at CT [12], [13].

Fig. 6(a) and (b) plot the measured recovered data eye diagram at 10 Gb/s at 300 and 4.2 K. The degradation of the eye-opening at CT is due to the loss and bandwidth constraints of long dipstick cables required for cryogenic measurements. Fig. 6(c) and (d) shows the recovered clock phase noise at 300 and 4.2 K, respectively, when the input data has a 10 Gb/s PRBS pattern of $2^{21} - 1$, the longest available in our instrument. The integrated rms jitter from 10 kHz to 1 GHz is 260 fs at RT and remains almost the same at 4.2 K as the AWG limits the in-band phase noise at both temperatures.

Based on the measured jitter transfer curves in Fig. 7(a), the CDR loop bandwidth is 54 and 40 MHz at 300 and 4.2 K, respectively. The jitter tolerance curves in Fig. 7(b) are measured by applying a PRBS9 as the input data using the AWG and measuring the BER by the Keysight M8046A. Each measurement point indicates the jitter amplitude at which the BER quickly increases from 10^{-12}. The jitter tolerance is 2 UIPP at a 5-MHz jitter frequency at 300 K and reduces to 0.85 UIPP at 4.2 K due to ISI caused by the long cables (∼2.5 m) from the CDR to the measurement instruments. Similar degradation is observed when the same-length cables are used to measure jitter tolerance at RT. At both temperatures, the CDR fulfills the mask requirement of the
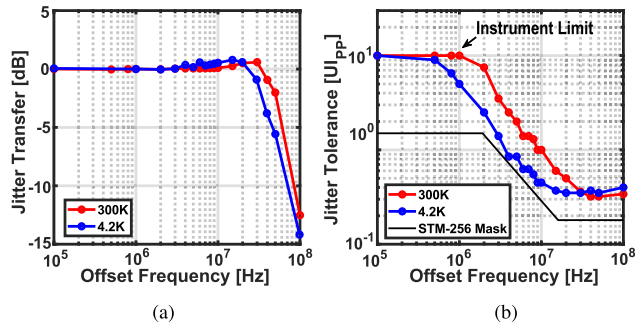
Fig. 7. Measured (a) jitter transfer and (b) jitter tolerance at 300 and 4.2 K.

TABLE I
COMPARISON WITH STATE-OF-THE-ART CDRs

	This Work		[5] JSSC'13	[6] JSSC'19	[14] JSSC'18	[15] JSSC'20
Architecture	Type-II PLL		Type-II PLL	Type-I PLL	Type-II AD-PLL	Type-II AD-PLL
Temperature [K]	300	4.2	300	300	300	300
Jitter Tolerance @ 5MHz [UIPP]	2	0.85#	0.7	2	1	0.35
Rec. Clock Jitter [ps]	0.260*	0.275*	1.5	0.459	1.46	1.15
Power [mW]	4.7	3.1	5	3	46	21.13
Efficiency [pJ/bit]	0.47	0.31	0.2	0.15	1.8	2.11
Data Rate [Gb/s]	10		25	20	25	10
Area [μm²]	130		39	0.36	50	31
Technology [nm]	40		65	45	40	28
Supply [V]	1.1		1	1	1.15	1
#measured over 2.5m cable *limited by instrument						

SDH STM-256 standard. Table I compares the proposed CDR performance with prior art NRZ CDRs. Thanks to the PD's simultaneous high gain, low power, and low jitter, this work at RT exhibits the lowest recovered clock jitter with competitive jitter tolerance and P_{dc}. Moreover, this work is the first CDR operating at CT, suited for QC applications.

IV. CONCLUSION

This letter introduced a CDR architecture demonstrating a low recovered clock jitter and high jitter tolerance thanks to incorporating a complementary charge sampling PD and clock alignment loop. The proposed 40-nm CDR operates at 10 Gb/s, achieving a recovered clock jitter of 275 fs (260 fs) and a jitter tolerance of 0.85 UI$_{PP}$ (2 UI$_{PP}$) at 5-MHz jitter frequency while consuming 3.1 mW (4.7 mW) at 4.2 K (300 K). As the first cryo-CMOS CDR, it enables the required data communication between classical and quantum processors in future large-scale quantum computers.

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